REMARKS

Claims 1-26 are pending in the application prior to entering this amendment.

The Examiner indicates allowability of claims 4-7, 13, 17-22, and 24-26 if rewritten in independent form including all of the limitations of the base and intervening claims.

The Examiner rejects claims 1-26 under the judicially created doctrine of double patenting over claims 1-29 of West (U.S. Patent No. 6,683,604).

The Examiner rejects claims 1-3, 8-10, 11-12, 14-15, 16 and 23 under 35 U.S.C. § 102(e) as being anticipated by Civanlar et al. (U.S. Patent No. 5,691,768).

The applicants amend claims 1, 11, 16, and 23.

The application remains with claims -- after entering this Amendment.

The applicants add no new matter and request reconsideration.

Claims Allowable

The applicants thank Examiner Nitin for his indication that claims 4-7, 13, 17-22, and 24-26 are allowable if rewritten in independent form including all of the limitations of the base and any intervening claims.

The applicants have amended the independent claims 1, 11, 16, and 23 and argue the allowability of all dependent claims below.

Double Patenting

The applicants enclose a terminal disclaimer to obviate the Examiner's double patenting rejections. The applicants note the present application is a continuation of U.S. Pat. No. 6,683,604 to West, both commonly owned by Pixelworks, Inc.

Claim Rejections Under § 102

The Examiner alleges Civanlar discloses a display system that discloses all of the elements recited. According to the Examiner, Civanlar discloses a system that includes a pixel packing circuit adapted to generate coded image data responsive to a failsafe enable signal and a pixel unpacking circuit adapted to generate output image data capable of being displayed on the display responsive to the failsafe enable signal, as recited in claims 1-3, 8-9, 11-12, 14-16, and 23. The Examiner concludes the invention recited is old in view of Civanlar.

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The Applicants disagree particularly as they amend the claims.

Claim 1 recites *a pixel packing circuit adapted to generate coded image data responsive to a failsafe enable signal, the coded image data... including a plurality of pixel bits and a palette bit, the palette bit to select one of a plurality of levels in a color palette for representing each of the pixel bits.* Claims 11, 16, and 23 include a similar limitation.

In an embodiment described in the specification, the failsafe circuit 102 compresses the input image generating coded image that includes plurality of pixel bits and an associated palette bit and then generates output image data by manipulating the coded image responsive to the palette bit. The system uses the palette bit to select one of a plurality of levels in a palette, as explained beginning at page 4. Nowhere does Civanlar disclose that its filtering and sub sampling circuit 105, the encoder 107, or the guard band 305 generate a plurality of pixel bits and a palette bit to select one of a plurality of levels in a palette as recited much less produce output image data based on manipulating the coded image data responsive to the palette bit.

CONCLUSION

The applicants request reconsideration and allowance of all claims. The applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Graciela G. Cowger
Registration No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

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